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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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William Edward Floro

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EXAMINER

RIOS CUEVAS, ROBERTO JOSE

ART UNIT

PAPER NUMBER

2836

DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application N .

10/058,959

Applicant(s)

FLORO ET AL.

Examiner

Roberto J Rios

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 January 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, and 6-19 is/are rejected.
- 7) ☒ Claim(s) 4 and 5 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 May 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 recites the step of unlatching the signal controlling the electronically controlled switch. Claim 12 fails to recite latching a signal controlling the electronically controlled switch. It is believed claim 15 depends from claim 14.

3. The following art rejection will be made as best understood by the Examiner in light of the above 35 USC 112 rejections.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, 12 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Caulkins (US patent 6,473,355).

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As per claims 1 and 12, Caulkins teaches a method of operating and a memory system having power backup comprising: a backup supply line receiving a backup voltage when a line voltage is lost; volatile memory receiving voltage from the backup supply line, the memory providing a low power operating mode controlled by volatile data held in the memory; and a voltage supervisory circuit communicating with the backup supply line and the volatile memory, wherein the backup supply line is disconnected from the volatile memory in response to a predetermined level in backup voltage below a normal backup voltage (col. 10, line 13; Figure 3A). Caulkins does not specifically disclose using a controllable switch to perform said interruption of backup power. However, a switching means is inherently used to selectively disconnect the supply of backup power from the memory.

As per claims 2 and 13, Caulkins teaches a backup voltage source connected to the backup supply line consisting of a battery (Figure 3A).

### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 3, 6, 9-11, 14-16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caulkins in view of Lee et al (US patent 4,730,121).

As per claims 3 and 14, Caulkins teaches disconnecting the battery from the memory but does not specifically teaches the claimed latching means. However, Lee et

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al (herein after Lee) teach a memory system including a latching means connected between a voltage supervisory circuit and an electronically controlled switch whereby the electronically controlled switch is latched to disconnect a backup supply line from the volatile memory even after restoration of backup voltage to the normal backup voltage while the memory system is not receiving line voltage (Figure 1; col. 11, line 40).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory system of Caulkins with the latching arrangement of Lee for the purpose isolating the battery from the memory and provide immunity form voltage spikes in the line voltage.

As per claim 15, Lee teaches unlatching the signal controlling the electronically controlled switch, thereby allowing reconnection of the backup battery to the volatile memory, after restoration of line voltage (col. 11, line 40).

As per claims 6 and 16, Lee teaches the voltage supervisory circuit receiving backup voltage (VL) from the backup supply line via the electronically controlled switch (Figure 1).

As per claims 9 and 19, Caulkins teaches the memory system but does not specifically disclose the claimed low power arrangement arrangement. However, Lee teaches a microprocessor communicating with the volatile memory; a low power warning circuit indicating a reduction of line power; and wherein the microprocessor executes a control program to read a low power warning signal from the low power warning circuit and in response to that signal to write to the volatile memory the volatile data to put the volatile memory into the low power operating mode (col. 8, line 21).

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It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory system of Caulkins with the low power arrangement of Lee for the purpose of putting the volatile memory into a low power battery backed operating mode.

As per claim 10, Caulkins teaches the backup voltage being from a battery but does not specifically disclose using a voltage converter between the battery and the volatile memory. However, the Examiner takes official notice that it is well known in the art to place a voltage converter between a backup battery and a volatile memory.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the teachings of Caulkins such that a voltage converter is placed between a backup battery and a volatile memory for the purpose of providing proper operating voltage to said memory.

As per claim 11, Caulkins teaches the volatile memory being DRAM (col. 17, line 53).

8. Claims 7, 8, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caulkins in view of Zandveld et al (US patent 4,841,474).

As per claims 7, 8, 17 and 18, Caulkins teaches the memory system but does not specifically disclose the claimed latching arrangement. However, Zandveld et al (herein after Zandveld) teach a microprocessor; latching means connected between a voltage supervisory circuit and the microprocessor to provide a signal to the microprocessor indicating that the backup supply line has previously been disconnected from the volatile memory even after the backup supply line has been reconnected to the volatile

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memory while the memory system is not receiving line voltage; whereby a control program executed on the microprocessor can determine after a power up the integrity of data in the volatile memory and said latch is reset after restoration or power (Figure 4; col. 9, line 53+; claim 1).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory system of Caulkins with the latching arrangement of Zandveld for the purpose of determining data integrity.

***Allowable Subject Matter***

9. Claims 4 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach or fairly suggest a memory system including a backup voltage selectively coupled to a volatile memory, wherein a latch means comprising a logic gate having at least one input tracking the output of a controlled switch is provided as in the claimed combination of elements recited in claim 4.

11. Art of general nature relating to memory and backup systems has been cited for applicant's review.

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**Communication with PTO**

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberto Rios whose telephone number is (703) 306-5518. In the event that Examiner Rios cannot be reached, his supervisor, Brian Sircus may be contacted at (703) 308-3119. The fax number for Before-Final communications and After-Final communications is (703) 872-9306.



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